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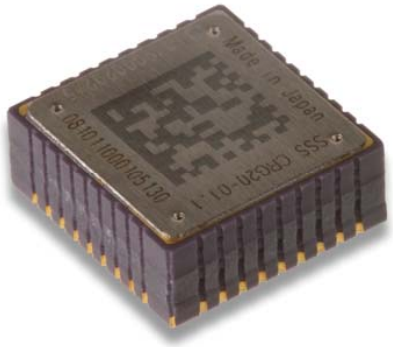
CRG20-12 High Rate Digital Angular Rate Sensor



GENERAL DESCRIPTION

CRG 20-12 is a high rate range (800 °/s) angular rate sensor and is part of the CRG20 family of MEMS rate sensors. The CRG 20 family is the latest evolution of angular rate sensor utilising Silicon Sensing's patented cos2θ ring structure MEMS technology. It is designed to meet the requirements of a wide range of automotive and commercial applications.

CRG20 builds upon the success of Silicon Sensing's benchmark family of MEMS rate sensors. Over 10 million of these have been delivered, with proven success in high performance automotive applications.

The sensor is a fully integrated digital solution, comprising MEMS sensing element, digital acquisition ASIC, and microprocessor. This single chip solution minimises the requirements for additional electronics, and thereby reduces space requirements and overall system costs. Fully digital closed loop control eliminates any temperature and ageing effects associated with analogue electronics, and provides exceptionally stable performance over a wide range of operating conditions.

The unique resonating ring structure makes the gyro inherently immune to high levels of shock and vibration, and eliminates problems with locking and static friction (known as 'stiction'), commonly experienced with other designs of coriolis MEMS sensors.

In addition to a commanded self test feature, CRG20 incorporates continuous self-testing of the complete operation of the sensor and the signal conditioning circuits. CRG20 has been designed to provide unparalleled sensor integrity, through the mitigation of potential error sources and false-plausible failure modes. System designers have the opportunity with CRG20 to eliminate the requirement for redundant sensors in high integrity applications.

The sensor provides a digital interface in the form of a SPI® port together with analogue output pins for customers who need to operate in the analogue domain. In addition, two auxiliary analogue input pins are available to digitise other sensors such as accelerometers or additional gyros; this enables multi-axis sensor clusters to be easily produced.

FEATURES

- Proprietary cos2θ ring MEMS technology
- Out of plane (z-axis) rate response
- No requirement for calibration
- Continuous comprehensive self test
- Suitable for high integrity applications
- High immunity to shock and vibration
- Ultra wide dynamic range
- 0.03125 °/s digital resolution
- Digital SPI® interface
- Compact LCC SMT package
- Two auxiliary ADC inputs
- Ratiometric analogue rate outputs
- Internal temperature sensor

APPLICATIONS

- Model Helicopters
- Robotics
- High rate Automotive
- High Agility AHRS / Navigation
- Event data recorders / telematics
- Machinery Control

ORDERING INFORMATION

Model	Bandwidth	Digital Rate Range	Analogue Rate Range
CRG20-12	40 Hz	800°/s	800°/s

The CRG20 family includes variants with a choice of bandwidth and rate range configurations. To discuss your requirements contact Silicon Sensing (contact information is detailed at the end of this document).

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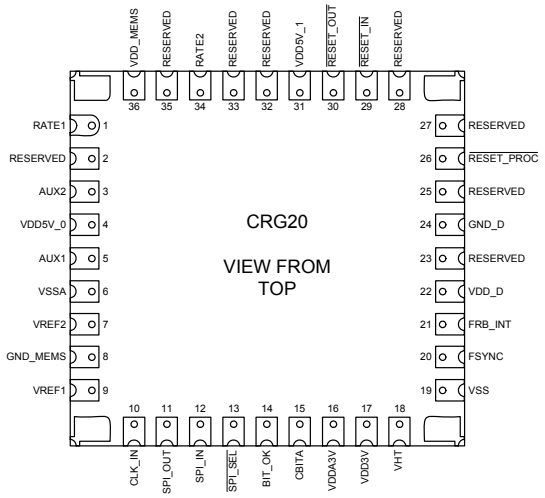

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ABSOLUTE MAXIMUM RATINGS

Operating Temperature	-40° C to +130° C
Storage Temperature	-60° C to +150° C
Maximum Operating Voltage	6.0V
Maximum Current on Start-up	75mA
Power Supply Ripple Requirement	<5mV pk-pk in frequency range 100Hz to 12 kHz <2mV pk-pk in frequency range 12kHz to 400MHz
Reverse Power Supply Protection	6V for 1 second with a current limit of < 100 mA

NOTE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or other conditions beyond those indicated is not implied.

NORMAL OPERATING RATINGS

Operating Temperature	-40° C to +105° C
Supply Voltage	5V dc nominal, (4.75V min, 5.25V max continuous)
Supply Current	60mA maximum @ 5.25V across operating temperature

ESD SENSITIVITY

The CRG20 device is rated to 2kV using the Human Body Model (direct contact, 100pF/1.5kOhm).

ESD (Electrostatic Discharge) Sensitive Device
This product may be damaged by ESD. Such damage may result in subtle performance or life degradation, or complete device failure. Appropriate storage and handling precautions should be taken at all times to avoid ESD damage.

FUNCTIONAL BLOCK DIAGRAM

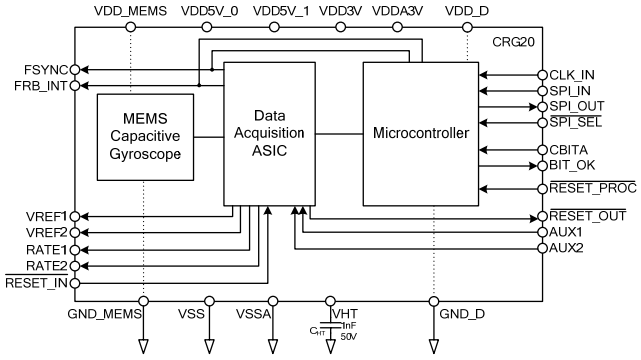

Figure 1

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CRG20-12 High Rate Digital Angular Rate Sensor

SPECIFICATIONS

Ambient Temperature (T_A) = -40°C to 105°C, V_{DD5V} = 4.75V to 5.25V, Angular Rate = 0°/s, unless otherwise stated.

Table 1

Parameters	Conditions	Units	Value *[1]
			CRG20-12
Digital Interface – Scale Factor			
Scale factor nominal		°/s/bit	0.03125
Full scale range		°/s	±800
Scale factor initial setting	T_A = 25°C	%	±0.50
Scale factor variation with temperature	Over full operating temperature range	%	±2.00
Scale factor rate linearity	Over full operating temperature range	% Full Scale	±0.15
Digital Interface – Bias			
Bias initial setting	T_A = 25°C	°/s	±0.50
Bias variation with temperature	Over full operating temperature range	°/s	±2.50
Bias switch on to switch on repeatability		°/s 1σ	0.07
g sensitivity (0±30 g range)		°/s/g	±0.10
g^2 sensitivity (0±30 g range)		°/s/g^2	±0.005
Bias hysteresis		°/s typ.	±0.1
Analogue Interface – Scale Factor			
Scale factor nominal	V_{DD5V} = 5.00V, ratiometric with V_{DD5V} supply	mV/°/s	2.5
Full scale range		°/s	±800
Scale factor initial setting	T_A = 25°C	%	±6.0
Scale factor rate linearity	Over full operating temperature range	% Full Scale	±0.15
Ratiometric error		%	1.0 max
Analogue Interface – Bias			
Bias initial setting	T_A = 25°C; V_{DD5V} = 5.00V, ratiometric with V_{DD5V} supply	V	2.5 ±0.015
g sensitivity (0±30 g range)		°/s/g	±0.10
g^2 sensitivity (0±30 g range)		°/s/g^2	±0.005
Analogue Inputs (Aux 1 shown, applicable to Aux2)			
Input dynamic range		V	V_{SSA} + 0.25 to V_{DD5V} – 0.25
Resolution	V_{DD5V} = 5.00V, ratiometric with V_{DD5V} supply	mV	1.22
Sample rate	Set to ¼ of the sensor frequency ~14kHz	kHz	>3.4
Integral nonlinearity		LSB	±8
Differential nonlinearity		LSB	±0.5
Offset error	Referred to pin AUX1 *[2], T_A = 25°C, V_{DD5V} = 5 V	mV	±32
Offset error stability over temperature and life	Referred to pin AUX1 *[2], V_{DD5V} = 5 V	mV	±10
Scale factor error	Referred to pin AUX1 *[2], T_A = 25°C, V_{DD5V} = 5 V	%	2.5
Scale factor error stability	Referred to pin AUX1 *[2], V_{DD5V} = 5 V	%	±0.7
Signal to noise and distortion ratio		dB	70
Noise	Referred to pin AUX1 *[2], up to 500 Hz	µV/√Hz	175
Input capacitance		pF	10
Input impedance		kΩ	50-300
Input bandwidth		Hz	500 *[3]
Analogue Rate Outputs			
Rate1		V	V_{REF1} ±2.3 max (±2.1 nom)
Rate2		V	V_{REF1} ±2.07 max (±1.89) nom
Rate1 resolution	V_{DD5V} = 5 V,	mV	1.123
Rate2 resolution	V_{DD5V} = 5 V, Rate1 x -0.9	mV	1.01
Rate1 & Rate2 offset error	With respect to V_{REF1}	°/s	±0.5
Rate1 & Rate2 offset error stability	With respect to V_{REF1}	°/s	±7
Rate1 & Rate2 scale factor error	With respect to V_{REF1}	%	±0.5
Rate1 & Rate2 scale factor error stability	With respect to V_{REF1}	%	±2.95
Rate1 & Rate2 reference voltage	Rate1 = Rate2 = V_{REF1} at 0°/s		V_{REF1}
Cross Coupling Errors			
Axis misalignment		mrad	±17
Axis misalignment stability		mrad	±8
Cross axis sensitivity		%	±2
Acceleration induced misalignment		mrad/(m/s^2)	0.2

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CRG20-12 High Rate Digital Angular Rate Sensor

Parameters	Conditions	Units	Value *[1]
			CRG20-12
Dynamic Response			
Gain peaking		dB	<1
Bandwidth	-3dB point	Hz	≥40
Angular acceleration limit		°/s²	>10,000
Noise			
Over 1 to 25Hz band		°/s rms typ.	0.20
In-band noise	Up to the bandwidth of the variant	°/s rms typ.	0.33
Over 1 to 101Hz band		°/s rms typ.	0.57
Broadband noise		°/s rms typ.	0.70
Angular random walk		°/√hr	>0.5 and <1
Commanded BIT (CBITA)			
Nominal rate output offset	T_A = 25°C	°/s	+10.0
Offset variation/tolerance	Between -40°C and 85°C	°/s	±3.00
Offset variation/tolerance	Between 85°C and 105°C	°/s	±3.75
Max data loss during test		ms	200
Power Supply			
V_{DD_D}		V	+5 ±0.25 *[4]
V_{DD5V_0}			
V_{DD5V_1}			
V_{DD_MEMS}			
V_{DD3V} *[5]		V	+3.3 ±0.2
V_{DDA3V}		V	+3.3 (15mA max)
V_{HT}	Generated internally by CRG20	V	+28 ±0.2
V_{DD} Quiescent supply current	V_{DD5V} = 5.25 V	mA	60
Voltage References			
V_{REF1}		V	V_{DD5V}/2 ± 0.25%
V_{REF1} Voltage offset error		mV	±14 max
V_{REF1} Voltage stability over temperature and life		mV	±7.5
V_{REF1} Load regulation	Sinking < 0.03mA into V_{REF1} pin, sourcing <1mA from V_{REF1} pin	%	±0.5
V_{REF1} Output noise	< 200 Hz < 20 kHz	mV rms	0.2 4
V_{REF1} Load capacitor required		nF	1 ±0.2
V_{REF2}		V	V_{DD5V}/3 ±1%
V_{REF2} Voltage stability over temperature and life		mV	±7.5
V_{REF2} Load capacitor required	Low ESR Tantalum type (0.1 – 0.5 Ω)	µF	10 ±2
Digital Signals			
Voltage level		V	5V CMOS logic
Input leakage current, I_{IN}		nA	50 max
Input capacitance, C_{IN}		pF	10 max
Start-Up			
Start-up time		ms	<500
Environment			
Temperature		°C	-40 to +105
Shock	½ sine, t = 2 ms, recovery within 20 ms	g	95 min
Vibration	20 Hz to 2 kHz	g rms	8.85
Mass		g	0.8
Mechanical Characteristics			
Package coefficient of thermal expansion		ppm/K	7.1

*[1] Unless otherwise stated errors quoted in this table refer to the digital rate output.

*[2] Where pin AUX1 is mentioned, the parameters are also applicable to AUX2.

*[3] The maximum measurable input bandwidth is limited by the communication scheme in the SERIAL PERIPHERAL INTERFACE PORT section, i.e. 500 Hz (half the maximum message rate).

*[4] Operating voltage stated as 4.75V-5.25V (5V optimum). Device to be connected as per Figure 3.

*[5] V_{DD3V} is generated internally, up to 15mA maximum draw load may be applied externally.

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PIN DIAGRAM

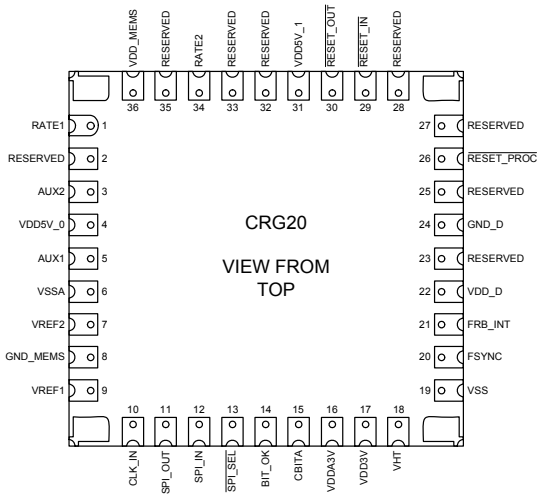

FIGURE 2

CRG20 PIN DESCRIPTIONS

Pin Name	Pin No	Pin Type[1]	Expected Value	Description
				Power Supply Connections
VDD5V_0	4	I	+5 V ±0.25 V	Analogue 5 V power supply connection 0. Used to power elements of the ASIC in the CRG20.
VDD5V_1	31	I	+5 V ±0.25 V	Analogue 5 V power supply connection 1. Used to power elements of the ASIC in the CRG20, including the charge pump for the high tension (HT) voltage. It is recommended that this connection be routed directly to the pin without passing through other power supply pins to minimise the effect of the charge pump operation on the CRG20.
VDD3V	17	I	+3.3 V ±0.2 V	3.3 V power supply connection for the ASIC. VDD3V does not need to be supplied with 3.3 V as the CRG20 contains an internal 3.3 V regulator.
VDDA3V	16	O	+3.3 V	Connection to the CRG20 internal 3.3 V regulator. This can be used to supply 3.3 V at currents up to 15 mA.
VDD_D	22	I	+5 V ±0.25 V	Digital 5V power supply connection for the microcontroller in the CRG20.
VDD_MEMS	36	I	+5 V ±0.25 V	Power supply connection for the MEMS and pickoff amplifier in the CRG20.
VHT	18	O	+28 V	Decoupling connection for the HT voltage charge pump in the CRG20. A 22 nF capacitor should be connected between VHT and VSS. Due to the sensitive nature of the HT voltage, the 22 nF capacitor should be on the same side of the mounting board as the CRG20 and the tracks should be as short as possible and not pass through any vias.
VSS	19	G	0 V	Ground connection for parts of the ASIC in the CRG20. It is recommended that the return path for this pin is not routed through any other ground pins, to minimise the effect of the charge pump operation on the CRG20.
VSSA	6	G	0 V	Ground connection for parts of the ASIC in the CRG20.
GND_D	24	G	0 V	Ground connection for the microcontroller in the CRG20.
GND_MEMS	8	G	0 V	Ground connection for the MEMS in the CRG20.
				Analogue Signals
AUX1	5	I	(VSSA+0.25 V) to (VDD5V-0.25 V)	External analogue input channel 1. The signal is digitised using a 12-bit analogue to digital converter (ADC) and can be observed using the SPI communications. See “Serial Peripheral Interface Port” section for details.
AUX2	3	I	(VSSA+0.25 V) to (VDD5V-0.25 V)	External analogue input channel 2. The signal is digitised using a 12-bit ADC and can be observed using the SPI communications. See “Serial Peripheral Interface Port” section for details.
RATE1	1	O	VREF1 ±2.3 V max	Buffered analogue output 1. This signal represents the angular rate applied to the CRG20 and is referenced to VREF1.
RATE2	34	O	VREF1 ±2.07 V max	Buffered analogue output 2. This signal represents the angular rate applied to the CRG20 and is referenced to VREF1. RATE2 is set to VSS if a continuous or demanded built in test (BIT) failure occurs.
VREF1	9	O	VDD5V / 2 ±7.5 mV	Analogue reference output 1. This output is used as the 0°/s reference for RATE1 and RATE2.
VREF2	7	O	VDD5V / 3 ±7.5 mV	Analogue reference output 2. VREF2 is used for internal referencing only and is brought out to a pin for the required decoupling. See “Recommended Layout” section for details.
				Digital Signals
BIT_OK	14	O	5 V CMOS Logic	The CRG20 performs continuous self checks and outputs the gross operational status of the device via the BIT_OK flag.
CBITA	15	I	5 V CMOS Logic	The CRG20 has the ability to initiate a commanded built in test. This can be done using the SPI communications (see “Serial Peripheral Interface Port” section for details) or the CBITA pin. CBITA is primarily used as a ‘quick test’ to check the functionality of the device. While CBITA is asserted, an offset is added to the rate sensing loop. BIT_OK shows a failure while CBITA is active.
CLK_IN	10	I	5 V CMOS Logic	SPI clock signal. This signal is typically a 1 MHz clock. See “Serial Peripheral Interface Port” section for details.
FRB_INT	21	O	5 V CMOS Logic	Frequency pulse output synchronous to the MEMS gyroscope resonant frequency. This signal will be in the range 3.35 kHz to 3.65 kHz. If the signal is used it should be buffered to reduce the

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Pin Name	Pin No	Pin Type[1]	Expected Value	Description
				risk of affecting the operation of the CRG20.
FSYNC	20	O	5 V CMOS Logic	Frequency output synchronous to 1024 times the MEMS gyroscope resonant frequency. This signal will be in the range 13.7216 MHz to 14.9504 MHz. If the signal is used it should be buffered to reduce the risk of affecting the operation of the CRG20.
RESET_IN	29	I	Active Low	When activated with an active low pulse, the ASIC is reset and 20µs later an active low reset signal is sent to RESET_OUT.
RESET_OUT	30	O	Active Low	RESET_OUT effectively mirrors the signal properties of RESET_IN with a 20µs delay. RESET_OUT is designed to be connected to RESET_PROC to reset the processor following an ASIC reset.
RESET_PROC	26	I	Active Low	When activated with an active low pulse, the processor is reset to initial conditions. The ASIC is not reset. The recommendation is to connect RESET_PROC to RESET_OUT so that the processor and ASIC are reset at the same time (effectively resetting the device). See "Recommended Layout section for details).
SPI_IN	12	I	5 V CMOS Logic	SPI data input (MOSI). See "Serial Peripheral Interface Port" section for details.
SPI_OUT	11	O	5 V CMOS Logic	SPI data output (MISO). See "Serial Peripheral Interface Port" section for details.
SPI_SEL	13	I	Active Low	SPI chip select. This line is active low. See "Serial Peripheral Interface Port" section for details.
				Miscellaneous Signals
RESERVED	2	-	0 V	Reserved for use by Silicon Sensing Systems Ltd. Should be tied to 0 V.
RESERVED	23	-	0V	Reserved for use by Silicon Sensing Systems Ltd. Should be tied to 0 V.
RESERVED	25	-	-	Reserved for use by Silicon Sensing Systems Ltd. Should be left unconnected
RESERVED	27	-	-	Reserved for use by Silicon Sensing Systems Ltd. Should be left unconnected
RESERVED	28	-	-	Reserved for use by Silicon Sensing Systems Ltd. Should be left unconnected
RESERVED	32	-	-	Reserved for use by Silicon Sensing Systems Ltd. Should be left unconnected
RESERVED	33	-	0 V	Reserved for use by Silicon Sensing Systems Ltd. Should be tied to 0 V.
RESERVED	35	-	-	Reserved for use by Silicon Sensing Systems Ltd. Should be left unconnected

[1] Pin types include: Input (I), Output (O) and Ground (G).

RECOMMENDED CIRCUIT DESIGN

Schematic

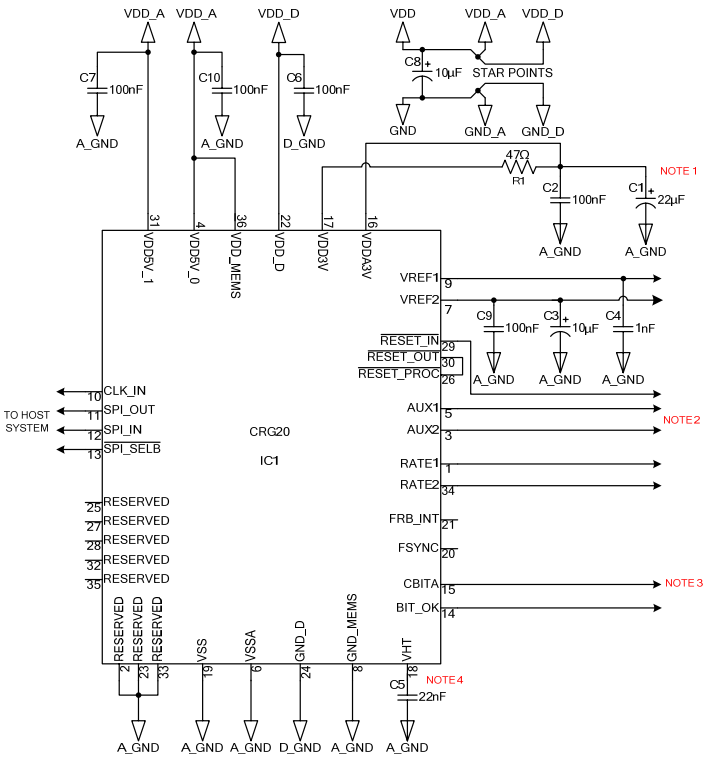

Figure 3

Bill Of Materials

No.	Ref. Des.	Value	Voltage	Tolerance	Package
1	IC1	CRG20	-	-	LCC-36
2	C1	22 µF	> 7 V	≤ 10 %	Case C
3	C2	100 nF	≥ 16 V	≤ 10 %	0603
4	C3	10 µF	≥ 16 V	≤ 10 %	Case B
5	C4	1 nF	≥ 16 V	≤ 10 %	0603
6	C5	22 nF	≥ 50 V	≤ 10 %	0603
7	C6	100 nF	≥ 16 V	≤ 10 %	0603
8	C7	100 nF	≥ 16 V	≤ 10 %	0603
9	C8	10 µF	≥ 16 V	≤ 10 %	Case B
10	C9	100 nF	≥ 16 V	≤ 10 %	0603
11	C10	100 nF	≥ 16 V	≤ 10 %	0603
12	R1	47Ω	≥ 16 V	≤ 1%	0603

Table 2

Schematic Notes

- Note 1: Capacitor C1 should be chosen to have an effective series resistance (ESR) of between 0.1 Ω and 0.5 Ω.
- Note 2: If the auxiliary inputs are not used they should be tied to a voltage between GND and VDD such as VREF1 (effectively mid-rail). This will prevent the AUX inputs causing ADC overflow errors which would result in a BIT failure.
- Note 3: Pin 15 (CBITA) of IC1 must be pulled down to GND to avoid the command BIT sequence triggering erroneously.
- Note 4: Pin 18 (VHT) of IC1 is an high impedance, high DC voltage signal and is sensitive to leakage currents. For this reason, the track connecting to C5 from pin 18 of IC1 should not contain any vias (i.e. the capacitor should be on the same side as the CRG20).

General PCB Design Notes

- IC1 is a ceramic package with a coefficient of thermal expansion (CTE) of 7.1 ppm/K. Board materials shall be chosen accordingly to minimise thermal mismatch.
- A ground screen is not shown to improve clarity. While a screening layer is beneficial, care must be taken to minimise copper as this increases the CTE of the board (see above). Hatched screens may be used to minimise this effect.
- ½ Ounce copper is recommended.
- If components are to be mounted on both sides of the board, care shall be taken to minimise the track lengths connecting decoupling capacitors to IC1, especially the capacitor C7 between pins 19 and 31
- The tracks labelled 'VDD' and 'GND' shall be connected to the system 5V and ground, respectively. Care shall be taken to minimise the resistance and inductance of these tracks, hence these tracks shall be as short as possible.
- The recommended package size for components has been chosen for ease of availability and is not restricted providing the values and tolerances are met.

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PCB Layout

The recommended PCB layout shown in Figures 4 to 9 has been tracked on 2 layers for simplicity. Higher numbers of board layers can be used for screening, although attention must be paid to the CTE of the package and matching it to that of the PCB material. Copper layers increase the CTE of FR4. Figure 4 shows the different Gerber data layers stacked together to represent the entire PCB.

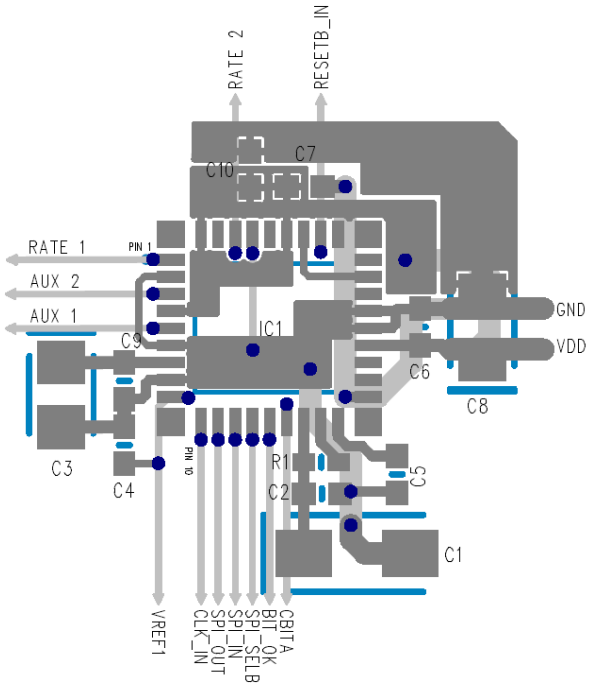


Figure 4

The recommended pad layout for the CRG20 36 pad LCC package is shown in Figure 5 and has been designed according to IPC 7351.

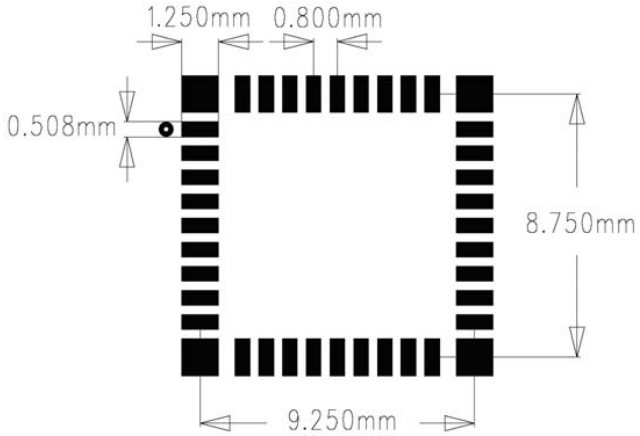
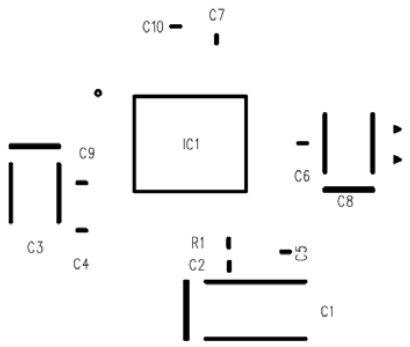


Figure 5

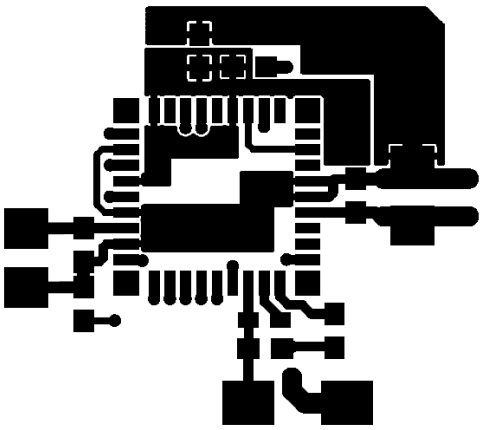
Top Silkscreen

Figure 6



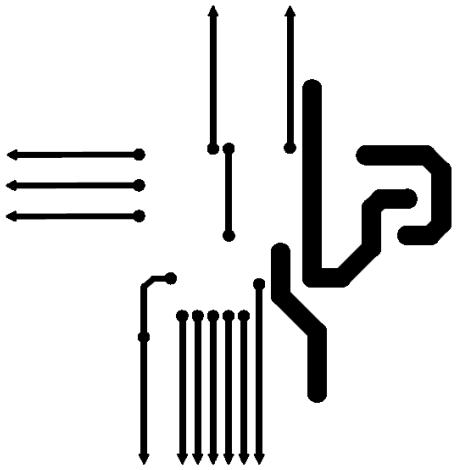
Layer 1 (Top) Copper

Figure 7



Layer 2 (Bottom) Copper

Figure 8



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THEORY OF OPERATION

The CRG20 uses a bulk silicon Micro-Machined ring structure, a mixed signal ASIC and a processor to make a single axis yaw rate sensor.

Principle

The Silicon ring is driven in a cos2θ mode shape to produce the radial velocity components required to make a Coriolis gyroscope.

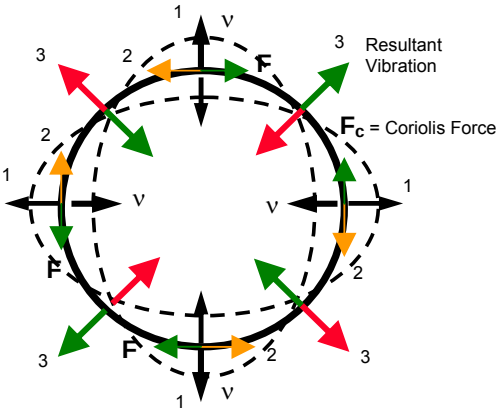

Figure 9

Figure 9 shows the movement of the silicon ring while vibrating:– As the ring oscillates in it's natural state the ring moves in the way shown by (1). When the gyro is turned, the Coriolis force acts on the ring as shown by (2). This causes a resultant vibration 45° out of alignment with the primary vibration, as shown by (3).The force required to completely null this resultant vibration is directly proportional to the angular rate.

Implementation

Eight uniformly spaced capacitive transducers are placed around the ring to form 2 pairs of drive transducers and 2 pairs of pickoff transducers.

One pair of diametrically opposed drive transducers is used to excite the cos2θ mode with the phase and amplitude sensed by the corresponding pickoff transducer pair. The drive amplitude and frequency is controlled by the ASIC and Processor to establish an accurate radial velocity component at the resonant frequency of the structure. This sets the basic operating point and scale factor of the system.

A secondary rate nulling loop is set up using the other drive and pickoff transducer pairs to enable the Coriolis forces (generated by applied angular rate) to be detected and servoed to zero using digital filters within the processor. This fully closed loop operation largely removes dependency of performance on the mechanical Q of the resonator and enables a very accurate level of bias and scale factor performance to be achieved without any compensation. The force required to null the coriolis force becomes an accurate measure of the applied angular rate.

All loop controllers and filtering are implemented within the processor so the rate (and other information) is available directly in digital form. This eliminates performance variation or drift in more typical analogue control loops, as the numeric control is inherently free from ageing, temperature and manufacture tolerances. All numeric processing is synchronised to the MEMS resonant frequency, so as to eliminate phase related detector errors commonly found in MEMS sensors.

The derived rate data is digitally filtered, scaled and then output via the SPI bus.

For legacy applications, the rate data is also converted to analogue format (with factory programmable scale factor and bias) and output on RATE1 and RATE2.

The digital rate data is output on the SPI interface together with other data (see SERIAL PERIPHERAL INTERFACE PORT) to produce a high integrity system

HIGH INTEGRITY RATE SENSING

A passive BIT system continuously monitors the health of the CRG20, incorporating the following techniques

Structure Integrity

The structure has been designed to 'fail silent' such that, in the unlikely event of the MEMS suffering mechanical damage, it will immediately stop vibrating as the changes in the mechanical tuning of the structure will cause significant change to the ring resonant frequency. Also, as there is only one interface to the structure, it isn't possible to lose part of it and continue to operate with reduced sensitivity.

System Node Observation

Due to the digital implementation of the control loops, every node can be monitored within the DSP code without additional complex circuitry or time delays. The subsequent reporting forms part of the standard payload of the SPI interface, available within every message, at one millisecond intervals

Analogue Feedback

The digital rate output is converted to an analogue voltage by passing through the internal SPI bus from the DSP to the ASIC. This value is converted in the same DAC as is used for force-rebalance. Two separate checks are now possible. Firstly, the analogue rate can be digitised by a host system, and compared with the rate as reported over the SPI bus. Secondly, this analogue signal can be connected to an auxiliary input of the same ADC as is used to monitor the transducers. It is redigitised within the sensor and presented to the host as an auxiliary data field in the SPI payload. Consequently, there are three measures of yaw rate that can be compared – providing triple verification.

DSP Verification

Conventional systems using a DSP have a residual failure mode whereby corruption of the arithmetic unit could cause the sensor to report an incorrect rate output with no means of internally validating the result. In CRG20, this is prevented by utilising time variant data to check for a predictable result to a test calculation. Using the low order byte of rate data from the previous message, a test calculation is run that exercises all of the operation types required to implement the control loop filters, and a packet of data is generated within the next SPI message payload (rate check byte). This is verified by the host, simply by implementing the same calculation, confirming the ALU integrity of both the CRG20 and the host.

COMMANDED BIT

The failure identification mechanisms described in the preceding sections operate continuously without interrupting or modifying the rate output. This is regarded as Continuous or Background Built In Test (BIT). There is also a commanded BIT, which is provided for backwards compatibility with legacy systems. In response to an external command, (either via the SPI interface or in response to a standard logic high level applied to the "CBITA" input), the secondary loop is disturbed to artificially invoke a fixed rate offset. This causes the output to change by a predetermined offset, which can be detected by the host system either via the SPI interface or via the analogue output.

SERIAL PERIPHERAL INTERFACE PORT

Communication with the CRG20 uses a serial peripheral interface (SPI) port, in which the CRG20 behaves as the slave. The SPI port includes four signals: SPI select (SPI_SEL), serial clock in (CLK_IN), MOSI or SPI data in (SPI_IN) and MISO or SPI data out (SPI_OUT). The SPI_SEL line enables the CRG20 SPI port and frames each communication. When the SPI_SEL line is high, SPI_OUT is held in a high impedance state and signals on CLK_IN and SPI_IN are ignored by the CRG20.
A communication consists of a 48-bit data frames split into 6 8-bit bytes. The SPI port operates in full duplex mode, which means that as data is transmitted to the CRG20 on SPI_IN, it is also received from the CRG20 on SPI_OUT.

Table 3 shows detailed timing information referenced from Figure 10 and Figure 11, which shows the detail of the SPI port data structure.

Table 3 - SPI Port Timing Information

Parameter	Min Value	Max Value	Unit	Description
t_{CLK}	0.8		µs	CLK_IN period.
t_1	5		µs	SPI_SEL to CLK_IN setup time.
t_2	0.4 x t_{CLK}		µs	CLK_IN high pulse width.
t_3	0.4 x t_{CLK}		µs	CLK_IN low pulse width.
t_4	1.1		µs	Delay between successive bytes.
t_Q	730		µs	Minimum quiet time required between SPI_SEL rising and start of next communication (Note 1)
t_h	0		µs	SPI_SELhold time after final clock
t_m	53.5	270	µs	message duration (note 1)
t_{tot}	1000		µs	repetition rate (Note 1)

Note 1: A quiet time (tq) between messages is required, and t1 + Tm + Th + tq = Ttot. Optimum performance is achieved with a repetition rate of 1ms. Select an appropriate Tclk to meet the requirements of Tm, and then adjust tq to give a Ttot of 1ms

EXTERNAL SYSTEM TO CRG20 MESSAGES

The data frames from the external system to the CRG20 are in the following format:

Byte	Function
0	Control Byte
1	Reserved
2	Reserved
3	Reserved
4	Reserved
5	Checksum

Control Byte:

RES	RES	RES	RES	CBITA	NMT2	NMT1	NMT0

bit 7 bit 0

bit 7-4 : **RES** : Reserved
Set to 0

bit 3 : **CBITA** : Commanded Built In Test A
0 = Deactivate CBIT_A test
1 = Activate CBIT_A test (see CBITA function)

bit 2-0 : **NMT2:NMT0** : Next Message Type
000 = Basic rate data (default)
001 = Rate /Aux1 sensor data
010 = Rate / Aux2 sensor data
011 = Rate / Temperature sensor data
100 = Device configuration 1 data
101 = Device configuration 2 data
110 = Reserved
111 = Reserved

Reserved:

RES	RES	RES	RES	RES	RES	RES	RES

bit 7 bit 0

bit 7-0 : **RES** : Reserved
Set to '00' hex

Checksum:

CHK7	CHK6	CHK5	CHK4	CHK3	CHK2	CHK1	CHK0

bit 7 bit 0

bit 7-0 : **CHK7:CHK0** : Checksum
1s complement of the sum of bytes 0 - 4

The checksum is the 1s complement of sum of the previous 5 bytes

CRG20 to External System Messages

The data frames transmitted from the CRG20 to the external system are in the following format:

Byte	Function
0	Status Byte
1	*Data 0*
2	*Data 1*
3	*Data 2*
4	*Data 3*
5	Checksum

Each message from the CRG20 begins with a status byte contained in byte 0 and a checksum in byte 5.

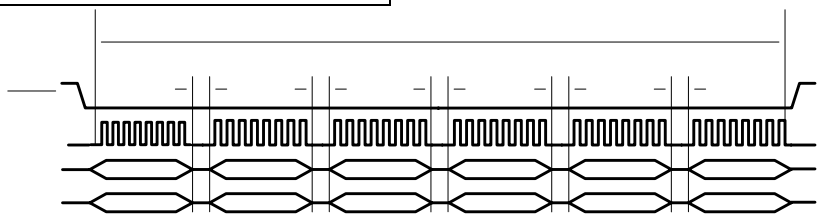

Figure 10 - SPI Data Frame Structure

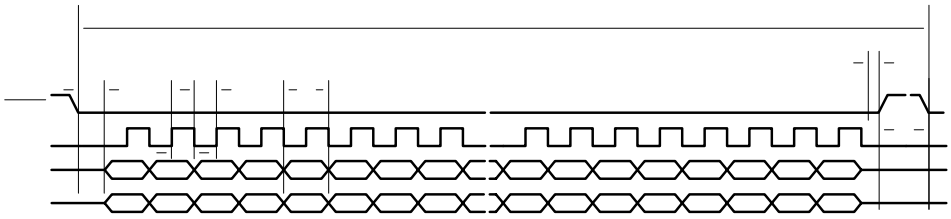

Figure 11 - SPI Data Timing Diagram

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Status Byte:

MC1	MC0	HCF	BF	CBITA	MT2	MT1	MT0

bit 7 bit 0

bit 7-6 : **MC1:MC0** : Message Count
Incremented by the CRG20 each time the host system takes a message.

bit 5 **HCF** : Host communications fault
0 = No fault detected
1 = Communications fault detected

bit 4 **BF** : Built in test (BIT) fault
0 = Gyro output OK
1 = BIT Failure

bit 3 : **CBITA** : CBITA active
0 = CBIT_A test inactive
1 = CBIT_A test in progress

bit 2-0 : **MT2:MT0** : Message type
000 = Basic rate data (default)
001 = Rate /Aux1 sensor data
010 = Rate / Aux2 sensor data
011 = Rate / Temperature sensor data
100 = Device configuration 1 data
101 = Device configuration 2 data

Checksum:

CHK7	CHK6	CHK5	CHK4	CHK3	CHK2	CHK1	CHK0

bit 7 bit 0

bit 7-0 : **CHK7:CHK0** : Checksum
1s complement of the sum of bytes 0 - 4

Depending on the message type requested in NMT2:NMT0 in the previous control byte from the host, the data bytes (*Data 3*: *Data 0*) in the subsequent data frame from the CRG20 contain the following data, indicated by NMT2:NMT0:

Basic Rate Data Message (NMT2:NMT0 = 000)

Byte	Function	Description
0	Status Byte	
1	Rate MS	Nominally ±850°/s, 0.03125°/s/lsb
2	Rate LS	
3	Rate Check Byte	See Page 9
4	Reserved	Reserved
5	Checksum	

Rate / Aux1 Message (NMT2:NMT0 = 001)

Byte	Function	Description
0	Status Byte	
1	Rate MS	Nominally ±850°/s, 0.03125°/s/lsb
2	Rate LS	
3	Aux1 MS	Aux1 data (signed integer), 1.22 mV/lsb
4	Aux1 LS	
5	Checksum	

Rate / Aux2 Message (NMT2:NMT0 = 010)

Byte	Function	Description
0	Status Byte	
1	Rate MS	Nominally ±850°/s, 0.03125°/s/lsb
2	Rate LS	
3	Aux2 MS	Aux2 data (signed integer), 1.22 mV/lsb
4	Aux2 LS	
5	Checksum	

Rate / Temperature Sensor Message (NMT2:NMT0 = 011)

Byte	Function	Description
0	Status Byte	
1	Rate MS	Nominally ±850°/s, 0.03125°/s/lsb
2	Rate LS	
3	Temperature MS	-50°C to 145°C, 0.125°C/lsb
4	Temperature LS	
5	Checksum	

Device Configuration 1 Message (NMT2:NMT0 = 100) – Default on power up

Byte	Function	Description
0	Status Byte	
1	Bits (7:4) Bits (3:0)	Model rate range (e.g. 3 = 75°/s) Model bandwidth (e.g. 1 = 100Hz)
2	Bits (7:4) Bits (3:0)	Spare bits Model variant
3	Software Version	Software variant number
4	Bits (7:5) Bits (4:0)	Spare bits Year of manufacture
5	Checksum	

Device Configuration 2 Message (NMT2:NMT0 = 101)

Byte	Function	Description
0	Status Byte	
1	Bits (7:4) Bits (3:0)	Month of manufacture (3:0) Package lot number (11:8)
2	Bits (7:0)	Package lot number (7:0)
3	Bits (7:6) Bits (5:0)	Assembly plant (1:0) Device serial number (13:8)
4	Bits (7:0)	Device serial number (7:0)
5	Checksum	

Note: The contents of the two device configuration messages give each sensor a unique serial number.

Note: If an incorrect message is received, the CRG20 will continue to transmit the message chosen in the last valid request. Upon power up, the CRG20 will output the device configuration 1 message until a valid control signal is received.

EXTERNAL INTERFACE DISCRETE SIGNALS

Two discrete signals are part of the external host interface of the CRG20:

CBITA (Input)

The CRG20 has the ability to initiate a commanded built in test. This is used as a test to ensure the device is functioning correctly, by exercising the CRG20 MEMS structure, the rate sensing loops and drive and pickoff electronics. CBITA works by applying an offset to the loops running inside the rate sensor, which results in a 10°/s offset bias in the rate output. The timing of the offset in relation to the state of the CBITA pin is shown in Figure 10.

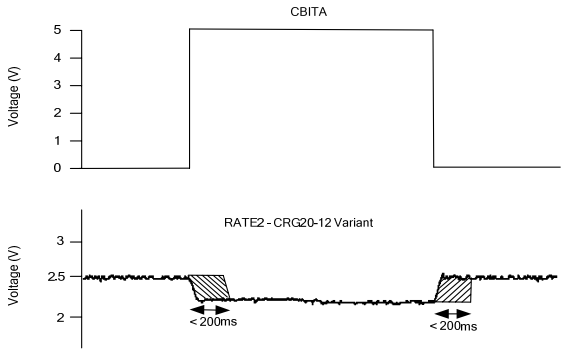

Figure 10 - CBITA Timing

CBITA Logic Levels

CBITA = 0 The CBITA test will be disabled.

CBITA = 1 The CRG20 will initiate a CBITA test, in which a nominal offset bias of 10°/s will be applied to the rate output.

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BIT_OK (output)

While operational, the CRG20 performs continuous self-checks during operation and outputs the gross operational state of the CRG20 with the BIT_OK flag.

The built in test (BIT) function is a comprehensive test of the sensor and the signal conditioning circuits. BIT_OK can take up to 500ms to show a valid rate output after the CRG20 is powered up, as shown in Figure 11.

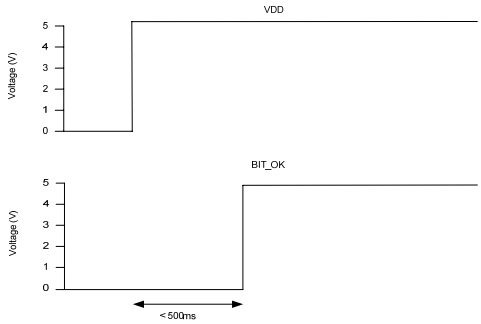

Figure 11 - BIT_OK Timing

During normal operation, the BIT_OK flag is set within 25mS of a fault condition.

BIT_OK Logic Levels

BIT_OK = 0	The rate output from the CRG20 is invalid, as the built in test has failed (or CBIT is running)
BIT_OK = 1	The rate output is valid.

RESET_IN (input)

The CRG20 has a discrete input which is capable of resetting the device. The RESET_IN input is an active-low signal. When pulled low for a minimum of 2µs, the ASIC in the CRG20 enters a reset state. If the RESET_OUT and RESET_PROC pins are connected, the ASIC will then also reset the processor in the CRG20. The timing of the reset sequence is shown in Figure 12.

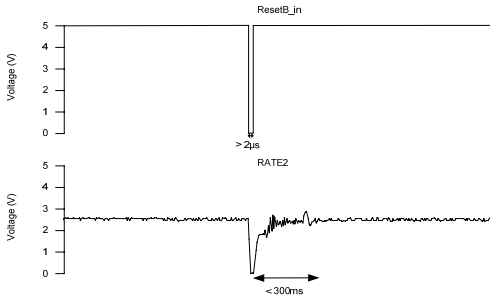

Figure 12 - RESET_IN Timing

RESET_IN Logic Levels

RESET_IN = 0	After a minimum of 2µs, the CRG20 is held in reset.
RESET_IN = 1	The CRG20 is in normal operation.

Auxiliary Input Channels

CRG20 has a pair of Auxiliary Analogue Inputs that are available to the user. These inputs are converted into digital format synchronised to the operation of the gyro. The data can be accessed as single packets for each input together with rate information.

The measurements can be read by the host system using the “Rate / Aux 1” and “Rate / Aux 2” message types (see page 11).

There are three constraints that the user needs to be aware of:
1. To maximise the fault detection capability of the sensor system, the inputs are checked for underflow and overflow. Therefore, it is essential to constrain the input signal between V_{SSA} + 0.25V to V_{DD5V} – 0.25V. Failure to do so will be interpreted as an invalid input signal and result in a logic ‘1’ in bit 4 of the Status byte. (**BF** : Built in test (BIT) fault)

2. The input impedance of the auxiliary channels lies between 50kOhm and 300 kOhm, with up to 10pF of input capacitance. It is therefore necessary to ensure that the input is fed from a source that has sufficiently low output impedance that the signal is not adversely attenuated by the aux input itself.

3. The Aux inputs are sampled and converted for a maximum data rate of 1kHz. Therefore, the input signal must be constrained to not exceeding 500Hz to prevent aliasing.

Analogue Rate Output Channels

There are two analogue rate outputs from the CRG20, RATE1 and RATE2. Both rate outputs are referenced to VREF1, bipolar (around VREF1) and directly proportional to the applied rate.

RATE1 has a minimum voltage range of ±2.1 V with respect to VREF1. When positive rate is applied, the voltage increases (within the rate limits of the gyro).

RATE2 is effectively the RATE1 output scaled by -0.9, giving it a minimum voltage range of ±1.89 V with respect to VREF1. When positive rate is applied to the CRG20, the RATE2 output voltage decreases (within the rate limits of the gyro).

The smaller voltage range used for RATE2 allows the signal to be used to show BIT failure. When a BIT failure occurs (with the exception of CBIT being asserted), the RATE2 output falls to within 0.1 V of VSS. During normal operation, the decreased voltage range means the output will never reach this level.

Voltage References

The CRG20 has two voltage reference outputs.

VREF1 is the 0°/s rate reference for the RATE1 and RATE2 analogue output channels. VREF1 is nominally (VDD5V – VSS) / 2. VREF1 has an offset error of no greater than ±14 mV.

VREF2 is used internally by the ASIC in the CRG20. It is nominally (VDD5V – VSS) / 3 and is only brought out to a pad as it requires decoupling (see RECOMMENDED LAYOUT).

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MECHANICAL DESIGN

Package Outline Dimensions

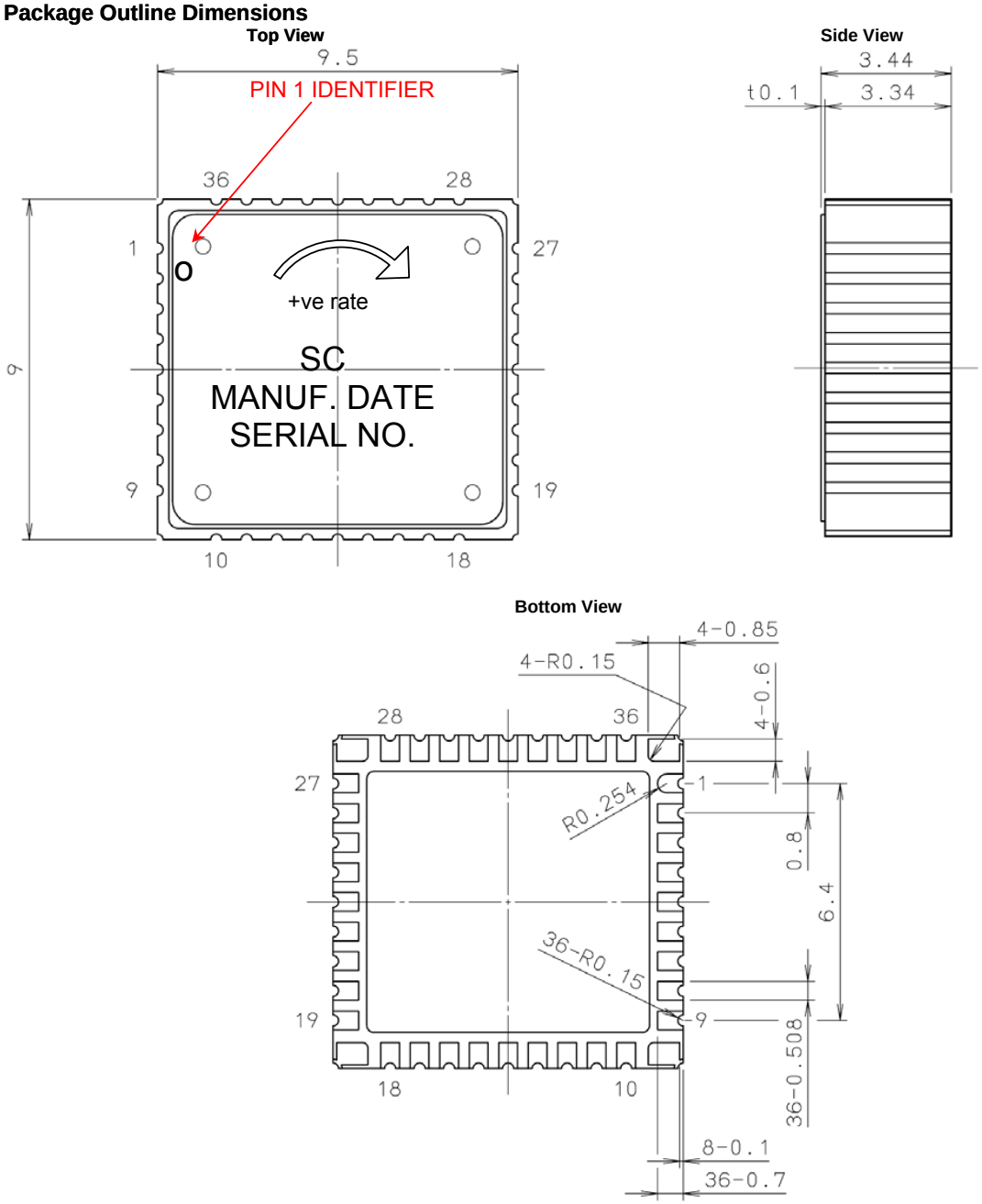

Figure 13 - Package Outline Dimensions

Alignment & Tilt Specification

In order to ensure the cross-axis sensitivity specification is met, the CRG20 should be mounted parallel to the board so that after soldering it has a tilt of 0.25° or less, with respect to the mounting surface.

Recommended Solder Conditions

The CRG20 is designed to be reflow soldered to a PCB. It is recommended that lead-free solder flow conditions should not exceed 235°C with a dwell over 220°C of less than 60 seconds. However, short duration dwells of 10 seconds or less at temperatures of up to 260°C can be tolerated.

Package Details

The CRG20 package is made from alumina high temperature co-fired ceramic (HTCC).

The pads on the CRG20 are electroplated with 5 µm of nickel, followed by up to 0.5 µm of electroplated gold.

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